REMARKS

Claims 1 to 8 are pending. Claims 1 to 8 are currently rejected. Reconsideration of the application is requested.

§ 103 Rejections

Applicants respectfully submit that according to MPEP 2142, to establish a case of *prima facie* obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) the prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co., 226 USPQ 438 (PTO Bd. App. 1984).*

Claims 1 and 4 were rejected under 35 U.S.C. 103(a) as being anticipated by Gregor et al. (US 5,354,955) in view of Hanson et al.(US 4,496,793).

The Office Action essentially states that:

Regarding claim 1, Gregor et al, discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

1. a substrate (12; column 3, line 7) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that define contact pads (the pads under the solder ball 20 and pads on the top surface of the substrate 12) for attachment to corresponding pads on the chip (14; column 3, line 8) and board (10; column 3, line 5),
2. wherein the board attach surface (at the bottom surface of the substrate 12) comprises
   - a pattern of contact pads (the pads under the solder ball 20) opposite and "adjacent" a chip attach location (the area on the substrate 12 where the chip 14 is attached) on the chip attach surface except at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of the board attach surface (see e.g., Fig. l),
   - said unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being "adjacent" to a comer of chip attach location (see e.g., Fig. l), and
3. said board attach surface (the surface that has the elements 120) comprising a dielectric material (the lowermost dielectric layer in the element 12). As shown in e.g., Fig 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region. Gregor et al. doesn't explicitly state that the unpatterned solid plane area is at least the size at which the strain is less then the cracking strain in the thermal cycling from 125°C to -55°C. The stresses are related

to the types of materials and other parameters i.e., the die size and thickness, substrate thickness, etc. (see page 12, lines 27 - 30 of the specification of instant invention), so in a device where a crack does not occur, it can be assumed that the size is greater than the size at which the strain causes a crack, as if it weren't then the crack would occur.

Mils SPEC Std 202 specifies that devices should operate without failures in solder joints from -55°C to +125°C. Therefore, one of ordinary skill would have found reason, motivation and suggestion to select the material so that no cracking occurs in cycling over the operating range of -55°C to +125°C. In designing a device to exceed the standard for Mil standard 202, the lack of cracking would inherently require the absence of cracking, which would mean for the size of the unpatterned area was large enough that no cracking accurs. Furthermore, it is a common knowledge that reducing thermal stress or thermal mismatch prevents cracking in the substrate (see column 7, line 66 - column 8, line 6 of Arai et al.).

To withstand common standard thermal stress cycles, the multi-layer board must withstand more than 400 thermal stress cycles to meet Mil Std 202. Inherently, any multi-layer board withstood the more than 400 thermal stress cycles per Mil Std 202 which is thermal cycling of assembled circuits between -55°C to +125°C with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles.

Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpatterned solid plane area being at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area is taught by Hanson et al. in e.g., column 4, lines 54 - 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to -55°C without cracking or failures. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the circuit board that withstands more than strain due to thermal cycling from 125°C to - 55°C without cracking or failures of Hanson et al. to be the substrate of Gregor et al. as taught by Hanson et al. to produce an average thermal coefficient of expansion of approximately $8.9 * 10^{-6}$ inch per inch per degree Celsius (column 4, lines 57 - 60).

Regarding claim 4, Gregor et al, discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

4. a substrate (12) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that defines a pattern of contact pads (the pads between the solder ball 20 and the substrate 12) for attachment to corresponding pads on the chip (14) and board (10),
5. wherein the board attach surface (at the bottom surface of the substrate 12) comprises
    - at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25),
    - said unpatterned area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being opposite a chip attach surface region adjacent at least one corner of a chip attach location (see e.g., Fig. l), and
6. said board attach surface comprising a metal (At the year 1994, all wirings or circuits or pads materials includes metal materials, i.e., copper or aluminum, etc. Thus, Gregor et al. anticipates this limitation.). As shown in e.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region. Furthermore, to withstand common standard thermal stress cycles, the multilayer board must withstand more than 400 thermal stress cycles per Mil Std 202. Inherently, any multi-layer board withstood the more than 400 thermal stress

> cycles per Mil Std 202 which is thermal cycling of assembled circuits between -55 and 125 degrees Celsius with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles.
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> Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpatterned solid plane area being at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area" is taught by Hanson et al. in e.g., column 4, lines 54 - 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to -55°C without cracking or failures. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the area of the circuit board that withstands more than strain due to thermal cycling from 125°C to -55°C without cracking or failures of Hanson et al. into the substrate of Gregor et al. as taught by Hanson et al. to produce an average thermal coefficient of expansion of approximately 8.9 * 10" inch per inch per degree Celsius (column 4, lines 57 - 60).

The Office Action states in part: "Gregor et al. doesn't explicitly state that the unpatterned solid plane area is at least the size at which the strain is less then the cracking strain in the thermal cycling from 125°C to -55°C. The stresses are related to the types of materials and other parameters i.e., the die size and thickness, substrate thickness, etc. (see page 12, lines 27 - 30 of the specification of instant invention), so in a device where a crack does not occur, it can be assumed that the size is greater than the size at which the strain causes a crack, as if it weren't then the crack would occur." (emphasis added) Applicants requests the Examiner to provide the basis on which the assumption is made that the absence of a crack in Gregor is achieved by the present invention rather than other solutions such as the internal metalized stabilizing layers of Hanson, which is cited by the Office Action.

The Office Action further states in part: "In designing a device to exceed the standard for Mil standard 202, the lack of cracking would inherently require the absence of cracking, which would mean for the size of the unpatterned area was large enough that no cracking occurs." Applicants initially point out that nothing in Gregor indicates that it is trying to exceed Mil standard 202, which is a military specification, so it would not be known if the device in Gregor would exceed Mil standard 202. Applicants also request the Examiner to provide the basis on which the determination was made that absence of cracking must be because an unpatterned area was large enough that no cracking occurs rather than because another solution was used.

Applicants also request that the Examiner provide a copy of Mil SPEC 202 because Applicants were unable to obtain a copy.

The Office Action further states in part: "Inherently, any multi-layer board withstood the more than 400 thermal stress cycles per Mil Std 202 which is thermal cycling of assembled circuits between -55 and 125 degrees Celsius with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles." Applicants would like to confirm that this portion of the Office Action is stating that any multi-layer board would inherently withstand 400 thermal stress cycles, and if so, ask the Examiner to provide the basis for this assertion, especially because nothing in Gregor indicates that it was trying to meet the requirements of Mil Standard 202.

Applicants respectfully submit that the references cannot support a case of *prima facie* obviousness as to the claims because, among other possible reasons, the cited references do not provide a motivation or suggestion for an unpatterned solid plane area on the board attach surface adjacent to a corner of a chip attach location, wherein the unpatterned solid plane area is at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area because the invention in Gregor is directed toward a multi-layer interposer in which the X-Y engineering change wiring pattern in the interposer terminates in a pattern of pads on the upper surface of the interposer around the periphery of the chip, and does not address thermal issues, cracking, etc., and Hanson teaches a means for addressing cracking problems that is an alternative to the present invention. Specifically, Hanson teaches the use of metal stabilizing layers inside the multi-layer circuit board, not on the board attach surface. *See* Hanson, e.g., at col. 3, lines 33-43. Furthermore, the stabilizing layers of Hanson are not a solid plane, but instead have enlarged apertures filled with epoxy resin. *See* Hanson, e.g., at col. 3, lines 44-48 and col. 4, lines 21-24. Therefore, the combination of the teachings of Hanson and Gregor still would not disclose or provide motivation for the present invention. Furthermore, there could be no reasonable expectation of success because neither references gives any indication that providing an unpatterned solid plane area on the board attach surface will inhibit cracking. In addition, these references do not disclose all the elements of the present invention because they do not disclose an unpatterned solid plane area on the board attach surface adjacent to a corner of a chip attach location, wherein the unpatterned solid plane area is at least the size of a region in which strain

due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area.

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims and request that the rejection be withdrawn.

Claims 2, 3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. and Hanson et al. as applied to claims 1and 4 above, and further in view of Lau (US 6,075,710).

The Office Action essentially states:

> Regarding claims 2, 3 and 5 - 7, while Gregor et al. and Hanson et al. disclose the use of the dielectric and metal materials on the board attach surface of the substrate, Gregor et al. and Hanson et al. do not disclose a solder mask on the dielectric material (claim 2) and metal (claim 6), the solder mask being a polyimide (claims 3 and 7) and the metal material being copper (claim 5). Lau teaches in e.g., Fig. 4A a solder mask (155 or 235; column 5, lines 65 - 67) on a dielectric material (the dielectric material in the bottom of the substrate; column 5, lines 19 and 20) and metal (Cu 130; column 5, lines 38 - 40) and the solder mask being a polyimide (column 7, line 39. Since the element 235 of Lau works as a mask layer for the solder pastes 245, the element 235 reads as a solder mask. Since the solder mask 235 is made by a polyimide material, Lau discloses a polyimide material for the solder mask). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the solder mask (e.g., polyimide) of Lau to cover the dielectric material and metal on the unpatterned solid plane area of Gregor et al. and Hanson et al. as taught by Lau to provide finer pitches between the external connections (column 6, lines 4 - 6).
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> Regarding claim 8, Gregor et al., as modified, discloses a solder mask (1 55 of Lau) having a plurality of openings (the openings for the pads 130 of Lau) defining ball grid array pads (see e.g., Fig. 3C).

Applicants incorporate by reference, their response above to the rejection of claims 1 and 4 based on Gregor in view of Hanson and submit that Lau does not make up for the deficiencies of Gregor and Hanson as prior art references.

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims and request that the rejection be withdrawn.

In addition to the foregoing arguments, Applicant(s) submit that a dependent claim should be considered allowable when its parent claim is allowed. *In re McCarn*, 101 USPQ 411 (CCPA 1954). Accordingly, provided the independent claims are allowed, all claims depending therefrom should also be allowed.

Based on the foregoing, it is submitted that the application is in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 103(a) is requested. Examination and reconsideration of the claims are requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant(s)' attorney if the Examiner believes any remaining questions or issues could be resolved.

Respectfully submitted,

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Date

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